

PCB Design and Verification Report

Four-camera GMSL2 carrier for a Jetson Orin NX module, 6 layers. Prepared by 1997circuits Engineering.

9.6 mV

module supply drop at 6 A, against a 50 mV budget

4 / 4

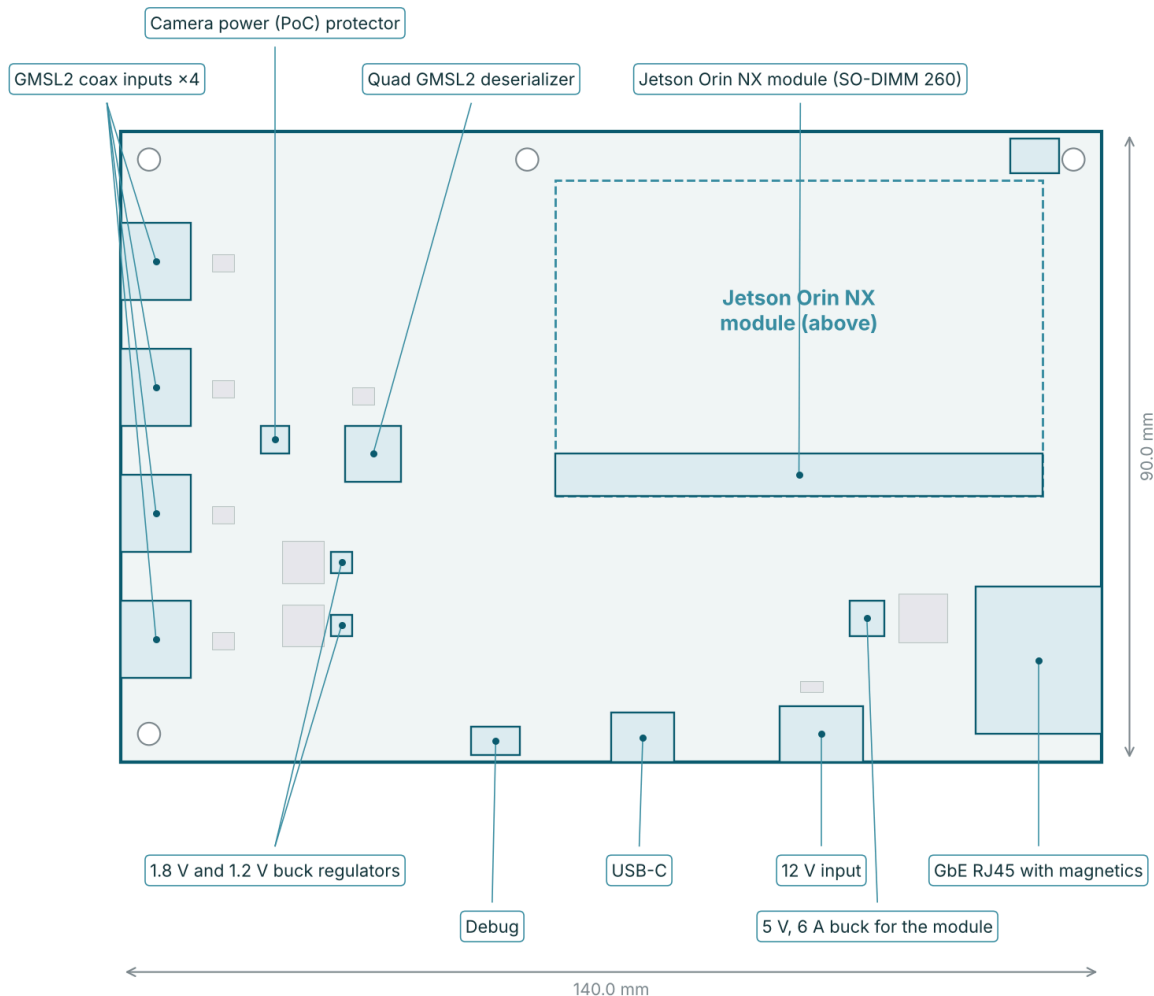
supply paths solved on the copper, all within budget

0.00 mm

P/N skew on all 9 differential pairs

0 crossings

CSI-2 bus nested, length-matched with serpentes

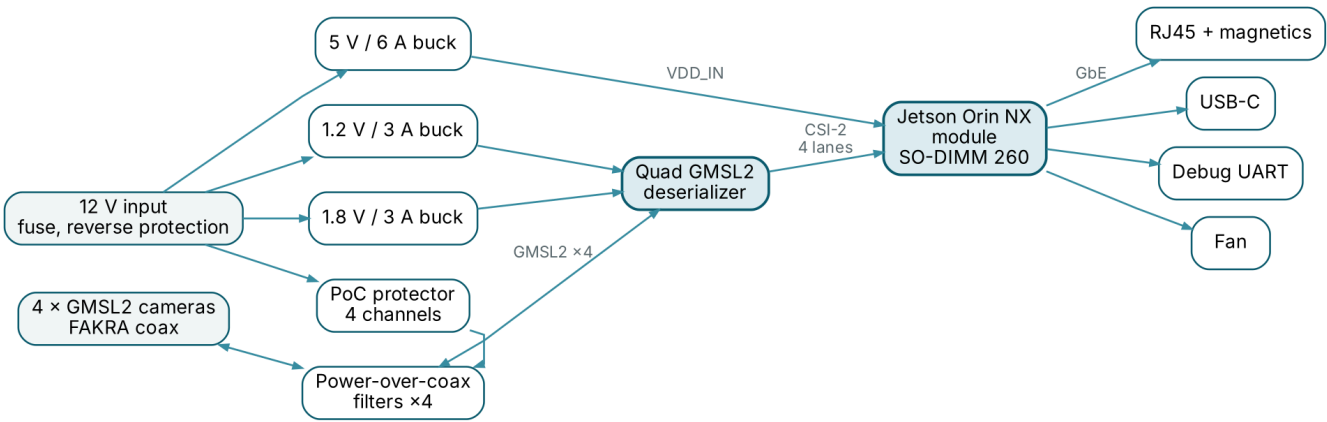


Placement, top side. The module sits on the SO-DIMM connector above the board.

About this sample. Illustrative sample on a 1997circuits concept board. Values are representative. The board pairs our own four-camera GMSL2 front end with a Jetson Orin NX module. Every figure, length and voltage drop in this report was computed on that concept layout; no customer design data is used.

1 Design overview

Four GMSL2 cameras come in on coax, with power sent up the same coax. A quad deserializer turns the four links into one MIPI CSI-2 port for the Jetson Orin NX module, which streams results out over Gigabit Ethernet. One 12 V input feeds everything.



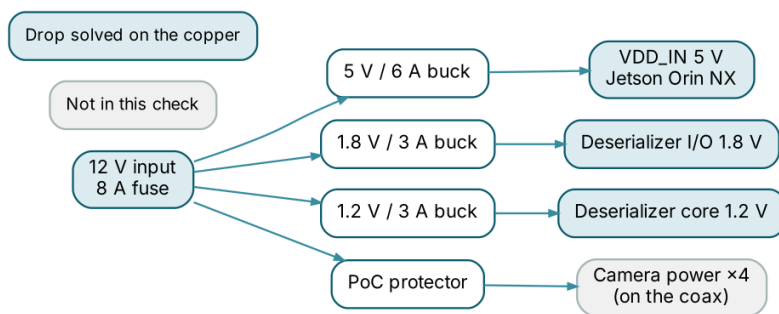
Functional blocks. Shaded blocks carry the high-speed and high-current paths checked in this report.

Area	How it is built	Result
Module supply (VDD_IN 5 V)	6 A buck next to the module connector, L4 pour to the SO-DIMM power pins	9.6 mV at 6 A, budget 50 mV. 11.8 mV at 85 °C
Deserializer supplies	1.8 V and 1.2 V bucks beside the deserializer, short L4 pours	Both within budget at the full 3 A buck rating (\$2)
CSI-2 to the module	4 data lanes and clock, 100 Ω stripline on L3, nested bus with serpentes	57.93 mm on every lane; P/N skew 0.00 mm
Gigabit Ethernet	4 MDI pairs, 100 Ω microstrip on L1, no vias, module to RJ45 magnetics	29.13 mm on every pair; P/N skew 0.00 mm
Camera links	50 Ω microstrip on L1 from each coax connector through its PoC filter	25.5 to 50.7 mm; clear of every part body
Stackup	6 layers, 1.6 mm, two unbroken ground planes	Widths set for 50 Ω and 100 Ω (\$4)

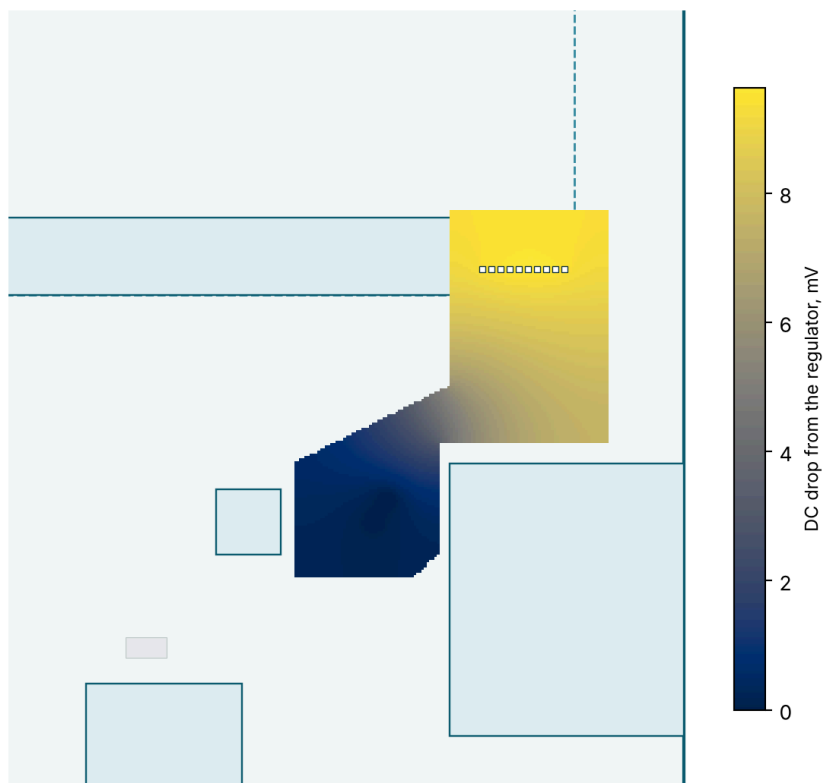
2 Power delivery

Design. Each supply is laid out so that the voltage lost in the copper between the regulator and the load stays inside a budget: 1 % of the supply voltage, 2 % for the 12 V input. The module supply runs on its own L4 pour and stops short of the RJ45 footprint.

Verification. A DC solve on each supply pour, with the regulator as the source and the load pins as sinks, at the regulator's full current rating (a stress case, above the expected load), at 25 °C and 85 °C.



Power tree.

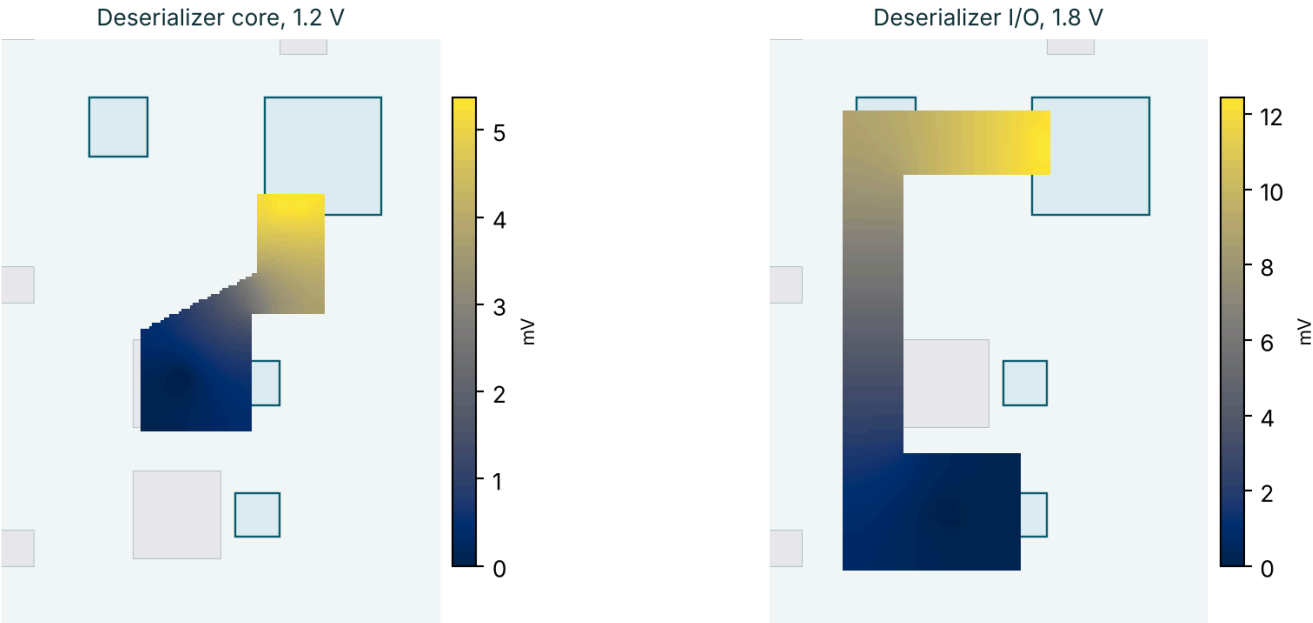


Module supply VDD_IN at 6 A on the L4 pour. Squares = SO-DIMM power pins. 9.6 mV at the worst pin, budget 50 mV.

2 Power delivery — supply paths

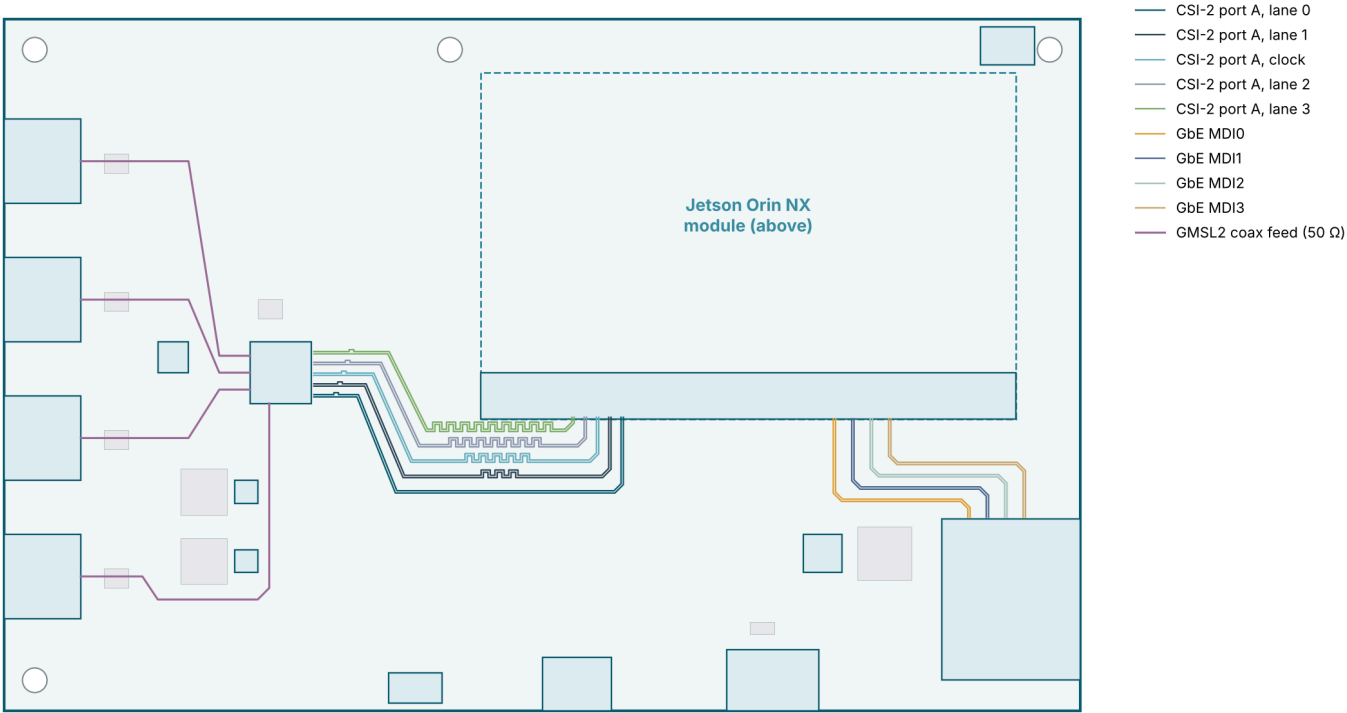
Supply	Path	Copper	Current	Budget	Drop 25 °C	Drop 85 °C	Within budget up to
VDD_IN 5 V	5 V buck to module power pins	L4, 1 oz	6 A	50 mV	9.6 mV	11.8 mV	31 A
1.2 V core	Buck to deserializer	L4, 1 oz	3 A	12 mV	5.3 mV	6.5 mV	6.8 A
1.8 V I/O	Buck to deserializer	L4, 1 oz	3 A	18 mV	12.4 mV	15.2 mV	4.4 A
12 V input	Input connector to the 5 V buck	L4, 1 oz	8 A	240 mV	10.5 mV	12.9 mV	183 A

Current = regulator or fuse rating. "Within budget up to" = budget ÷ path resistance at 25 °C: the current at which the path would use its whole budget.



Deserializer supplies at 3 A each. The 1.8 V pour wraps around the 1.2 V pour on the same layer; it is the longer path and has the smaller margin (4.4 A against 3 A).

3 High-speed routing

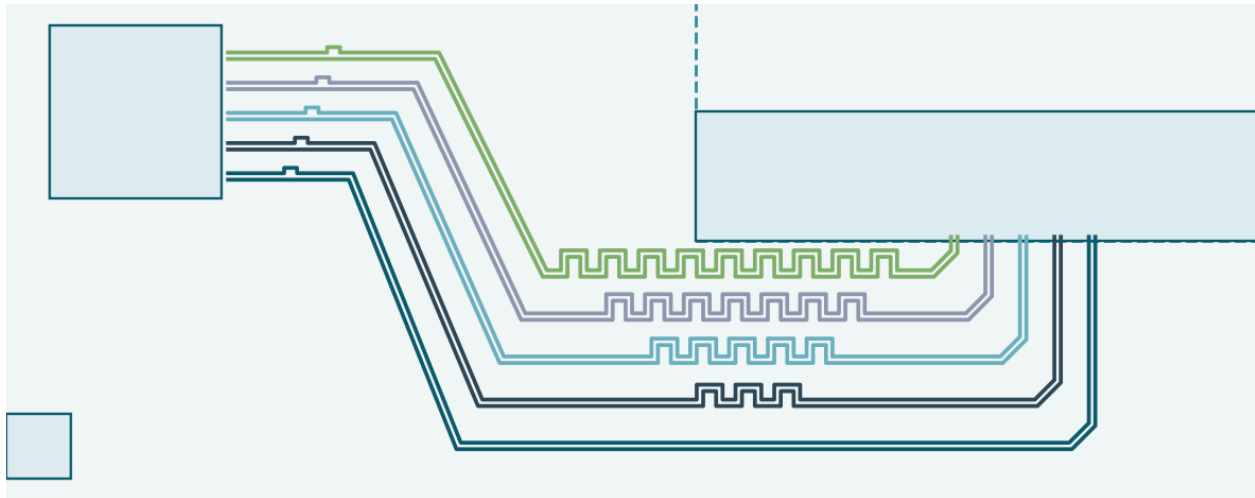


Routed high-speed nets. CSI-2 runs on L3 under the module; Ethernet runs on L1 from the module connector to the RJ45.

Interface	Pair	Layer	Vias	P (mm)	N (mm)	P/N skew (mm)
MIPI CSI-2, port A	Clock	L3 stripline	2	57.93	57.93	0.00
	Lane 0	L3 stripline	2	57.93	57.93	0.00
	Lane 1	L3 stripline	2	57.93	57.93	0.00
	Lane 2	L3 stripline	2	57.93	57.93	0.00
	Lane 3	L3 stripline	2	57.93	57.93	0.00
Gigabit Ethernet	MDIO	L1 microstrip	0	29.13	29.13	0.00
	MDI1	L1 microstrip	0	29.13	29.13	0.00
	MDI2	L1 microstrip	0	29.13	29.13	0.00
	MDI3	L1 microstrip	0	29.13	29.13	0.00

Lengths measured on the drawn copper, connector pin to connector pin. Lane-to-clock skew on CSI-2 is 0.00 mm.

3 High-speed routing — CSI-2 detail



CSI-2 escape from the deserializer (left) to the module connector (right). The lowest run turns up furthest right, so the bus never crosses itself; the shorter lanes take serpentine to reach the clock length.

Matching rules applied

Rule	Limit	Achieved
CSI-2 P/N, each pair	$\leq 0.05 \text{ mm}$	0.00 mm
CSI-2 lane to clock	$\leq 0.50 \text{ mm}$	0.00 mm
Ethernet P/N, each pair	$\leq 0.10 \text{ mm}$	0.00 mm
Serpentine leg spacing	$\geq 3 \times \text{width (0.45 mm)}$	0.45 mm
CSI-2 pair-to-pair spacing	$\geq 3 \times \text{width (0.45 mm)}$	0.66 mm

Camera links (single-ended, 50 Ω)

Link	Route	Length (mm)
A	Coax, PoC filter, around the buck stage	50.73
B	Coax, PoC filter, deserializer	25.46
C	Coax, PoC filter, deserializer	28.31
D	Coax, PoC filter, deserializer	43.61

GMSL2 links are independent, so these need no matching to each other; each stays short and on L1 over unbroken ground.

4 Stackup and impedance

	Layer	Used for
L1	Signal	GbE pairs (100 Ω), camera coax feeds (50 Ω)
	Prepreg 0.10 mm	
L2	Ground	Unbroken reference for L1 and L3
	Core 0.20 mm	
L3	Signal	CSI-2 lanes (100 Ω stripline)
	Prepreg 0.75 mm	
L4	Power	12 V, VDD_IN 5 V, 1.8 V, 1.2 V pours
	Core 0.20 mm	
L5	Ground	Reference for L4 and L6
	Prepreg 0.10 mm	
L6	Signal	I2C, GPIO, low-speed

6-layer stackup, 1.6 mm finished, symmetrical about the centre prepreg.

Build	FR-4 (Dk 4.0), 6 copper layers, 1 oz, 1.6 mm finished
Reference	L2 and L5 are unbroken ground; every high-speed pair runs over one of them
Power	All supply pours on L4, with 0.5 mm splits between rails

Net class	Layer	Target	Width / gap (mm)
Camera coax feed	L1	50 Ω	0.18
Ethernet MDI	L1	100 Ω diff	0.14 / 0.16
CSI-2	L3	100 Ω diff	0.15 / 0.15

Pre-layout widths from closed-form estimates; the fabricator's field solver confirms them on the ordered material.

Appendix — method

Lengths	Summed segment by segment along each drawn trace, including serpentine and skew-compensation bumps, from pin to pin. P and N are measured separately.
DC drop	2-D finite-difference solve of each pour on a 0.2 mm grid. 1 oz copper (34.8 μm) = 0.495 m Ω per square at 25 $^{\circ}\text{C}$, $\times 1.23$ at 85 $^{\circ}\text{C}$. Source = regulator output; sinks = load pins sharing the current equally.
Margin	"Within budget up to" divides the budget by the solved path resistance, so it reads directly as current headroom.

What you get with a 1997circuits layout review: a report like this one on your own routed board — drop maps, pair tables and stackup check — before the Gerbers go to the fab.

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