

Schematic Review Report

Four-camera GMSL2 deserializer board, rev A. Prepared by 1997circuits Engineering.

1 critical

camera power bypassed the protector and loaded all four links

1 major

protector exposed pad had no ground or thermal connection

4 of 4

findings closed, checked again in the release files

147 nets

connectivity check on the release files: 0 errors

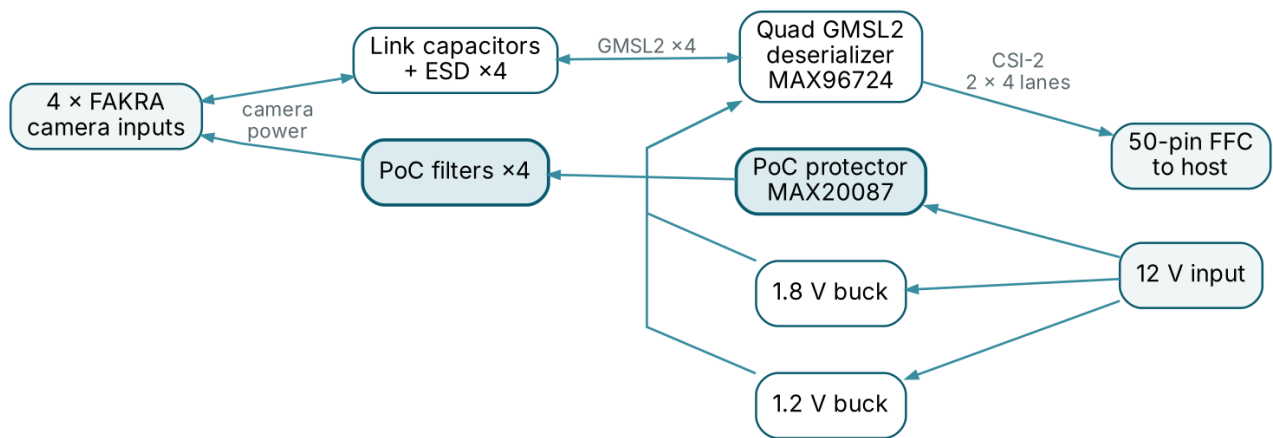
Findings

ID	Severity	Finding	Where	Status
F1	CRITICAL	Camera power bypasses the PoC protector, and the protector outputs with their 1 μ F capacitors sit on the coax node. No link would come up, and a shorted cable would draw straight from the 12 V rail.	U3 OUT1–4, C62–C65, L1–L4	Closed
F2	MAJOR	The protector symbol has no exposed pad, so the pad has no net: no ground and no heat path.	U3 symbol	Closed
F3	MINOR	Per-channel current limit is set by R29 but not written on the sheet.	R29 (ISET)	Closed
F4	MINOR	The open-source reference design's license notice is missing from the title blocks.	All sheets	Closed
N1	NOTE	Status-LED switch for the 1.2 V rail is driven below the gate voltage its datasheet specifies.	Q4, D19	Owner's call

About this sample. This is a real review of a 1997circuits board, our own four-camera GMSL2 design, shown the way we deliver it: the draft we were given, what we found and why, and the check of the release files after the fixes. Schematic extracts are from our board; no customer design data is used.

1 Scope and method

The board takes four GMSL2 cameras on coax, sends 12 V camera power up the same coax through a protected power-over-coax (PoC) stage, and hands the video to a host as two 4-lane MIPI CSI-2 ports on a 50-pin FFC.



Board blocks. Shaded blocks carry finding F1.

What we reviewed

Design	Native Altium project: 4 sheets, 213 components, 571 pins, 147 nets
Intent	The board's design guide: power budget, PoC current limit, host pin map
References	Datasheets of every active part, read at the pin and equation level

What we checked

Connectivity	Netlist built from the native files: multi-driver nets, unconnected pins, sheet-entry binding, designators
Power	Regulator setpoints, current ratings, protection path, default states at power-up
Interfaces	GMSL2 link coupling, CSI-2 lane map, I2C addresses, control pins and pull-ups
Records	Notes, settings and license notices a later engineer will need

Severity

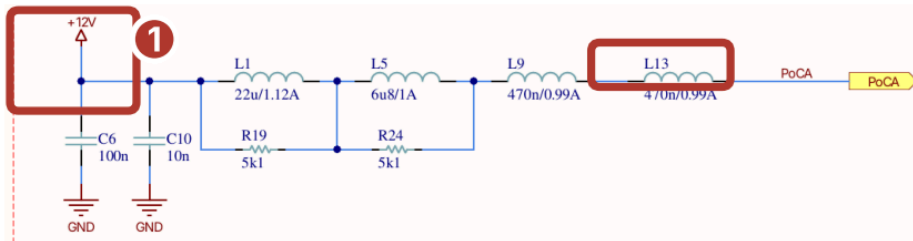
Level	Meaning
CRITICAL	Will not work, or causes damage. Fix before layout.
MAJOR	Likely failure or reliability risk in a stated condition. Fix before layout.
MINOR	Margin, compliance or robustness gap.
NOTE	Observation; no change required.

How each finding is written

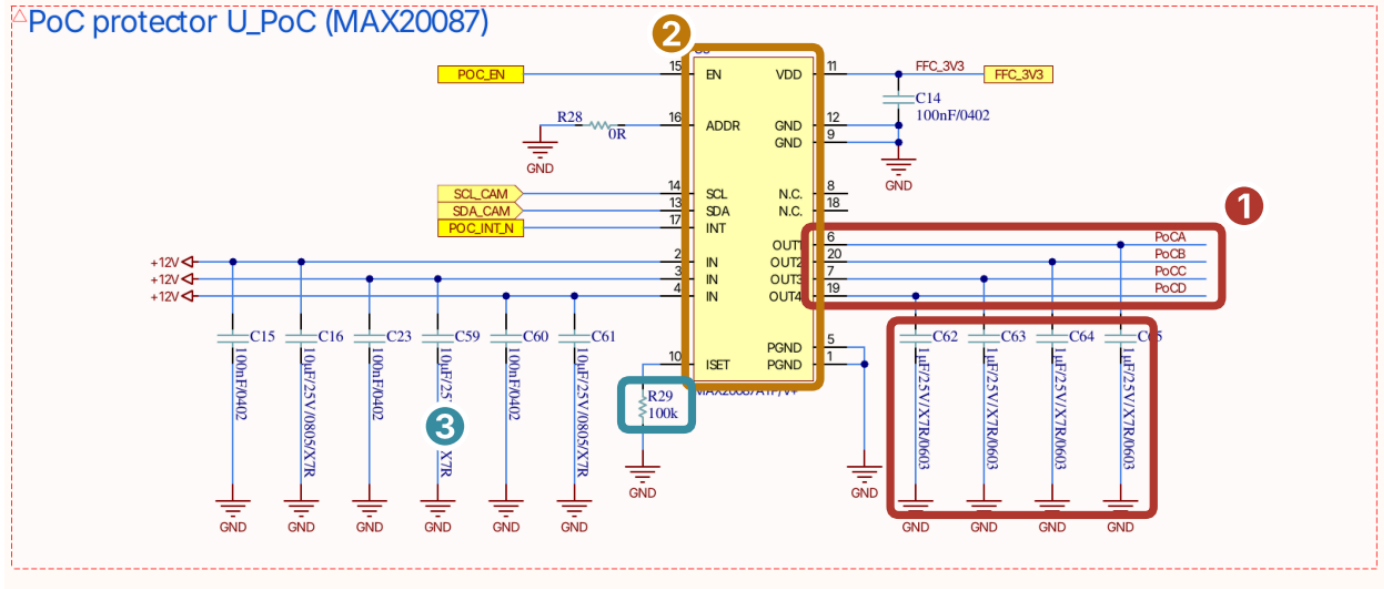
What we saw, with designators and nets; why it matters, with the datasheet line or engineering rule behind it; the fix; and how we confirmed the fix in the release files.

2 Findings

F1 **CRITICAL** Camera power bypasses the protector and loads the links



Draft schematic as submitted for review (power sheet, extract)



Draft, power sheet. ① 12 V feeds the top of each PoC chain, and the protector outputs land on PoCA–PoCD at the coax end together with C62–C65. ② The protector symbol stops at pin 20. ③ R29 sets the current limit, with no note.

What we saw

+12 V drives the top of all four PoC filter chains directly (C6–C13, L1–L4). The protector outputs OUT1–OUT4 are tied to PoCA–PoCD, the coax end of each chain, together with their 1 μ F output capacitors C62–C65.

Why it matters

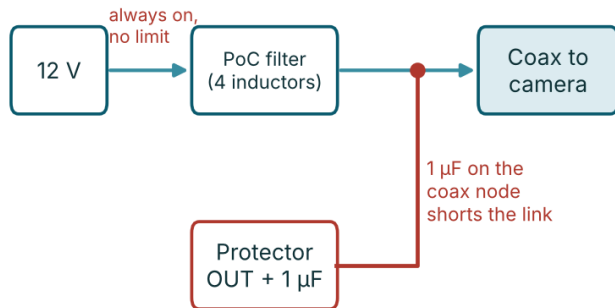
No protection: camera power never passes through U3, so its enable, its 600 mA current limit and its fault output do nothing; a shorted camera cable draws straight from the 12 V rail.

No video: the PoC filter must look like an open circuit to the 6 Gbps link and its back channel. A 1 μ F capacitor on the coax node shorts both, so none of the four links would lock.

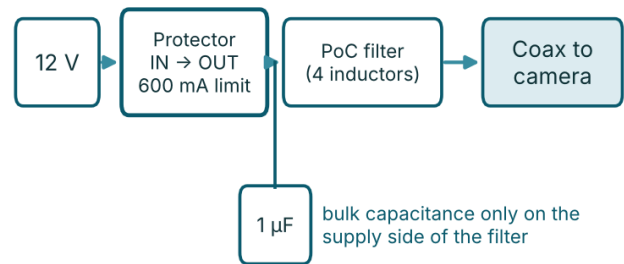
Back-drive: the 12 V rail also drives each protector output through the filter.

Datasheet (MAX20087, pin description): OUT is the protected camera supply output and takes a 1 μ F or larger ceramic capacitor to PGND. IN connects to the converter that feeds the cameras.

Draft: protector bypassed



Release: protector in the path



F1 in one picture: where the protector and its capacitor sit, before and after.

Fix 12 V to the protector IN pins only. Each OUTn to the top of its own chain (link A: the C6, C10, L1, R19 node, and so on). C62–C65 move with their outputs. Nothing but the filter on the coax side.

Confirmed Release files: each output now sits on the top of its own chain, for example OUT4 on net D with L4, R22, C9, C13 and C65 (pin 1 to GND). 0 multi-driver nets.

F2 MAJOR Protector exposed pad has no net

What we saw The U3 symbol has pins 1–20 only. The package has an exposed pad, but it is not in the symbol, so in layout the pad carries no net (see ② in the F1 figure).

Why it matters The datasheet ties GND and PGND to the exposed pad and asks for a grid of vias into the ground planes to carry the heat. Up to four channels at 600 mA pass through this package. With no net on the pad, nothing in layout or DRC will flag a missing thermal path.

Fix Add the exposed pad as pin 21 (EP), tie it to GND, and give the footprint pad a via grid.

Confirmed Release symbol has 21 pins including EP; EP is on GND (not in the unconnected-pin list).

F3 MINOR Current-limit setting not written down

What we saw R29 = 100 kΩ on ISET, with no note of what it sets (③ in the F1 figure).

Why it matters From the datasheet equation, $I_{LIM} = 600 \text{ mA} \times R_{ISET} / 100 \text{ k}\Omega = 600 \text{ mA per channel}$ ($\pm 8\%$: 552–648 mA). It is right, and it sits below the PoC inductor ratings (0.99–1.12 A). Without a note, a later "harmless" change to R29 moves the limit silently.

Fix · confirmed Note "600 mA per channel → R29 100 kΩ 1 %" placed next to U3. **Present in the release files.**

F4 MINOR Reference-design license notice missing

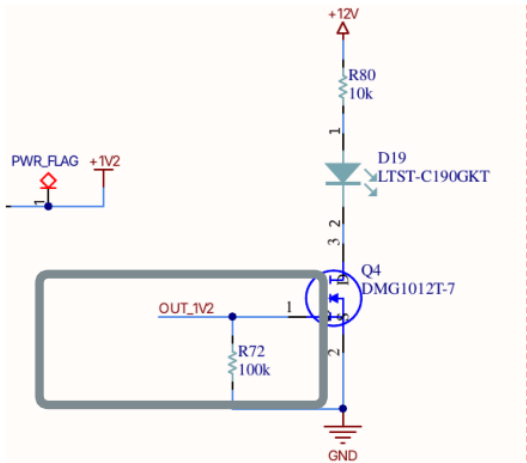
What we saw The board is derived from an open-source GMSL2 deserializer reference design (Apache-2.0). The title blocks do not say so.

Fix · confirmed One attribution line in every title block. **Present on all four sheets in the release files.**

N1

NOTE

Status LED switched from the 1.2 V rail



Q4 gate is the 1.2 V rail itself.

What we saw	Q4 (DMG1012T) switches status LED D19 from 12 V through R80 (10 kΩ). Its gate is driven by the 1.2 V output.
Why it matters	The FET's threshold can be as high as 1.0 V, and its on-resistance is specified only down to 1.8 V gate drive. At about 1 mA of LED current a typical part turns on, but brightness is not guaranteed on a worst-case part.
Options	A FET specified at 1.2 V gate drive, or keep as is: the LED is an indicator only and nothing else depends on it.

3

Checked and correct

A review also records what is right, with the numbers, so the next revision does not have to check it again.

Item	Calculation or evidence	Result
1.8 V buck setpoint	$0.8\text{ V} \times (1 + 12.4\text{ k}\Omega / 10\text{ k}\Omega) = 1.792\text{ V}$	Within 1.8 V $\pm 5\%$
1.2 V buck setpoint	$0.8\text{ V} \times (1 + 4.99\text{ k}\Omega / 10\text{ k}\Omega) = 1.199\text{ V}$	Within 1.2 V $\pm 5\%$
PoC limit vs filter rating	Worst-case limit 648 mA against inductors rated 0.99–1.12 A	$\geq 1.5\times$ margin
Camera power at start-up	Protector EN pulled down (100 kΩ): cameras stay off until the host enables them	Safe default
Protector fault output	INT is open-drain, pulled up (10 kΩ) to the host 3.3 V	Correct
Protector supply and address	VDD from host 3.3 V with 100 nF; ADDR to GND through R28 (0 Ω)	Correct
Link coupling	0.1 μF link capacitors on all four links, the GMSL2-mode value	Correct
Coax termination	The unused N side of each link ends in 49.9 Ω through 100 nF, as a coax link needs	Correct
CSI-2 to the host	Port A and port B, 4 data lanes + clock each, mapped to the FFC pin by pin	Consistent
Status-LED current	$(12\text{ V} - \sim 2\text{ V}) / 10\text{ k}\Omega \approx 1\text{ mA}$	Correct (see N1)

4 Re-check on the release files

After the fixes we rebuilt the netlist from the release files and checked every finding again, against the files themselves rather than a PDF print.

Findings

ID	Check in the release files	Result
F1	Each protector output on the top of its own PoC chain; 12 V only on IN	Closed
F2	Symbol pin 21 = EP, on GND	Closed
F3	Current-limit note next to U3	Closed
F4	Attribution line on all four sheets	Closed
N1	Left to the owner	Open

Connectivity

Check	Result
Sheet entries bound to ports	78 / 78
Multi-driver nets	0
Duplicate or unannotated designators	0
Unconnected pins	19, all intended

The 19: 13 unused FFC pins, 4 alternate MIPI clock pins not used in this lane mode, 2 pins marked N.C. by the manufacturer.

Appendix — method

Netlist	Built from the native schematic files (wires, junctions, net labels, power ports, sheet entries), not from a PDF, so hidden connections and missing pins show up.
Datasheets	Each finding cites the datasheet section or the engineering rule it rests on. Equations are worked with the values on the sheet.
Re-check	Every finding is closed against the release files themselves, with the evidence listed.

What you get with a 1997circuits schematic review: a report like this one on your own design, with findings ranked by severity, the evidence behind each, and a recommendation for every finding.

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